**Lab 6: Synchronous Counters**

**ITI 1100 C – Digital Systems 1**

**Winter 2016**

**School of Electrical Engineering and Computer Science**

**University of Ottawa**

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Submission Date: 2016-04-05

**Lab 6: Synchronous Counters**

**Objectives**

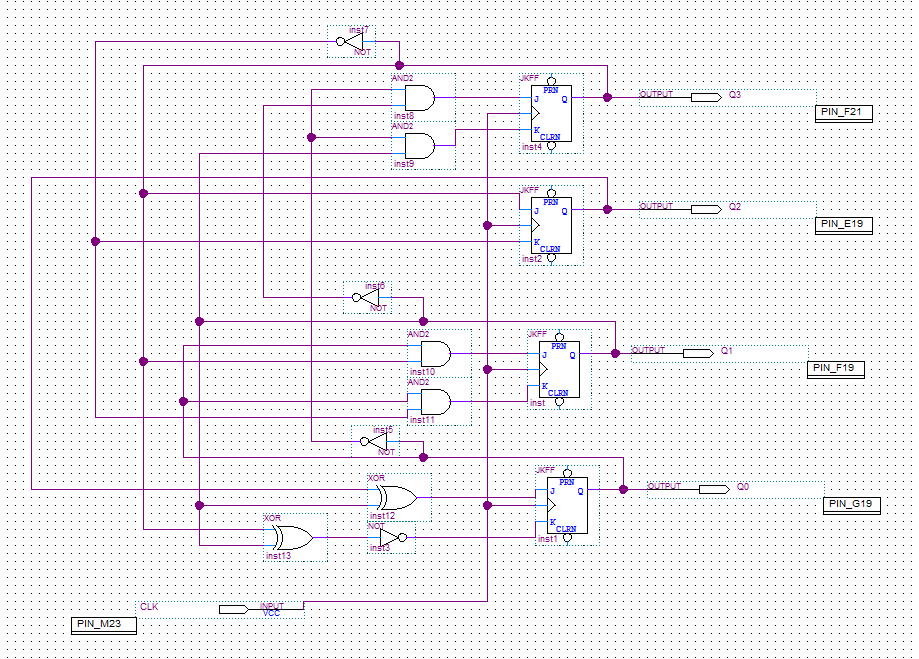
* Design synchronous counters
* Simulate the functions of the various counters in this laboratory exercise
* Display counter outputs as binary values on LEDs and test these counters

**Equipment and Components**

* Quartus II 13.0 Service-Pack 1 Software (64-bit)
* Altera DE2-115 circuit board

**Circuit Diagrams**

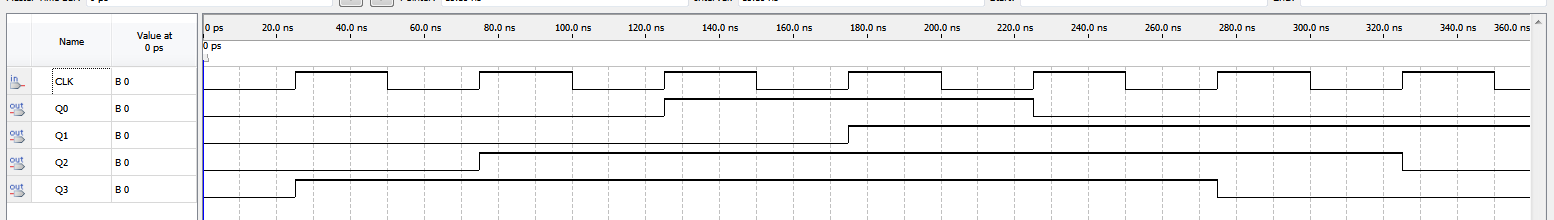
**A 4-Bit Synchronous Counter Diagram**

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**Figure 1:** Screen-shot of a 4-bit synchronous counter diagram.

**Experimental Data and Data Processing**

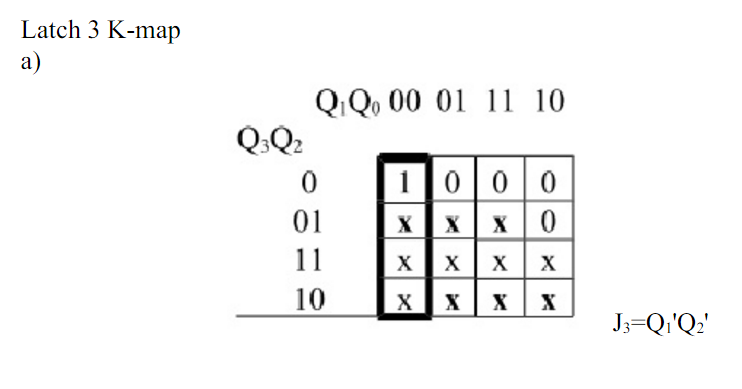
**A 4-Bit Synchronous Counter Diagram**

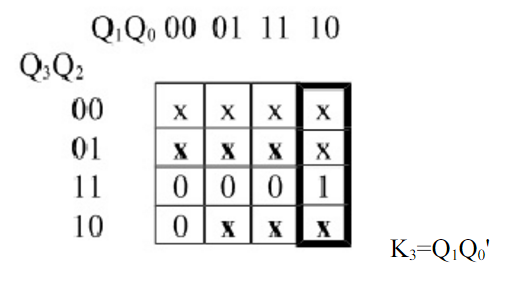


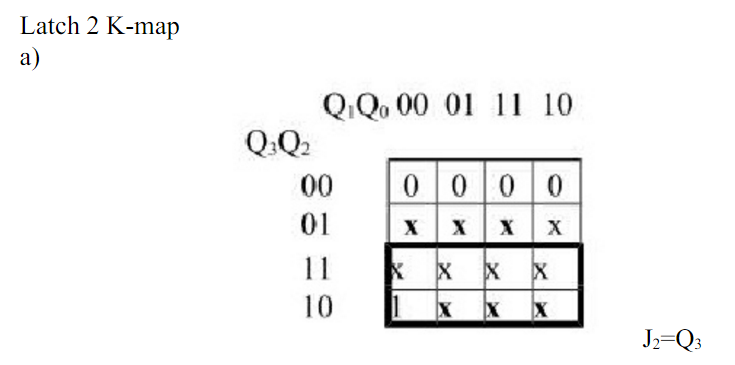
**Figure 1.2:** Screen-shot of the simulation output of the 4-bit Synchronous Counter Diagram.

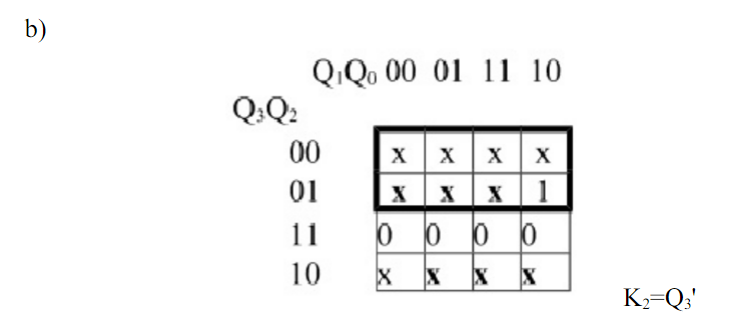
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **PS** | | | | **NS** | | | | **Q3** | | **Q2** | | **Q1** | | **Q0** | |
| **Q3** | **Q2** | **Q1** | **Q0** | **Q3\*** | **Q2\*** | **Q1\*** | **Q0\*** | **J3** | **K3** | **J2** | **K2** | **J1** | **K1** | **J0** | **K0** |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | x | 0 | x | 0 | x | 0 | x |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | x | x | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | x | 0 | x | x | 0 | 1 | x |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | x | 0 | x | x | x | x | 0 |
| 0 | 1 | 0 | 0 | x | X | x | x | x | x | x | x | x | x | x | x |
| 0 | 1 | 0 | 1 | x | X | x | x | x | x | x | x | x | x | x | x |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | x | x | 1 | x | 0 | 0 | x |
| 0 | 1 | 1 | 1 | X | x | x | X | x | x | x | x | x | x | x | x |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | x | 0 | 1 | x | 0 | x | 0 | x |
| 1 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 0 | 1 | 1 | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | x | 0 | x | 0 | 0 | x | 1 | x |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | x | 0 | x | 0 | 1 | x | x | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | x | 1 | x | 0 | x | 0 | 0 | x |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | x | 0 | x | 0 | x | 0 | x | 1 |

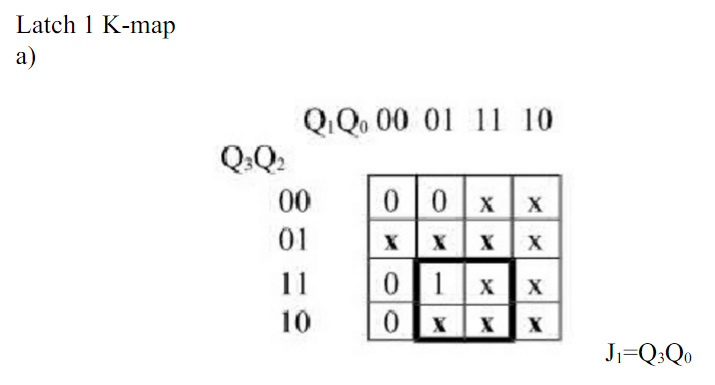
**Table 1:** From the corresponding K-maps, we can obtain the equations of the synchronous inputs as follows.

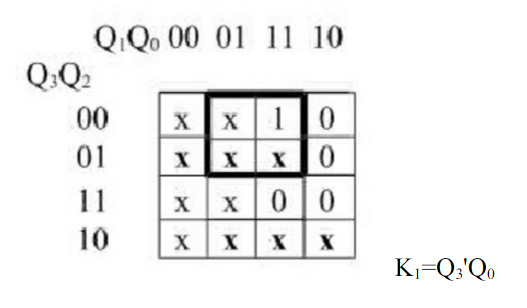
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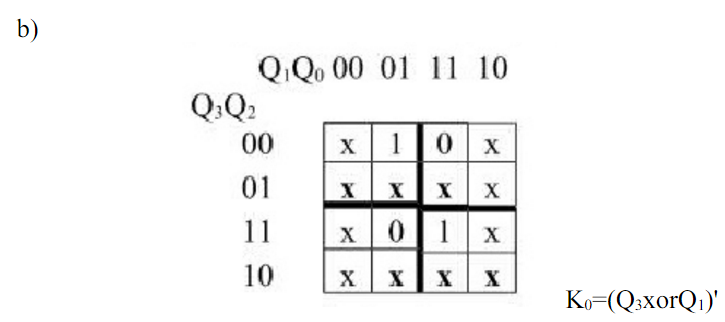
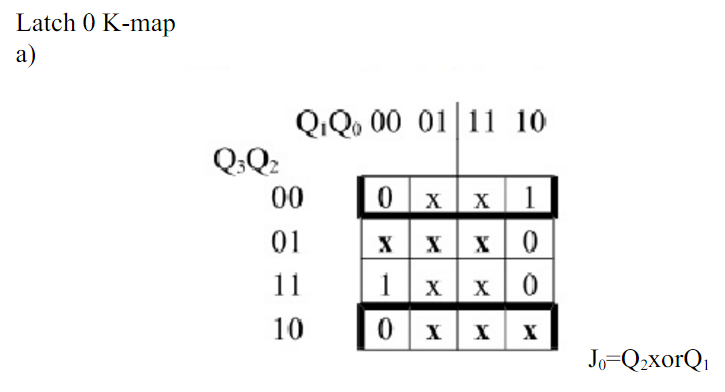
****b)

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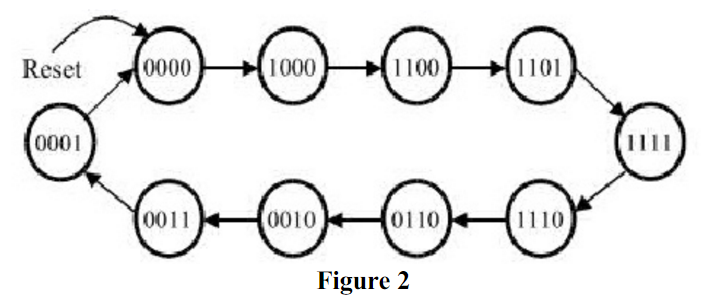
b)

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**Comparison of Theoretical Data and Experimental Data**

**A 4-Bit Synchronous Counter Diagram**

The process 4-bit synchronous counter designed in this experiment can be illustrated by the following state diagram, which has the same function as the state table previously shown.



In this experiment, the simulation results can be demonstrated by the following table.

|  |  |
| --- | --- |
| **Present State(Q3Q2Q1Q0)** | **Next State(Q3\*Q2\*Q1\*Q0\*)** |
| 0000 | 1000 |
| 1000 | 1100 |
| 1100 | 1101 |
| 1101 | 1111 |
| 1111 | 1110 |
| 1110 | 0110 |
| 0110 | 0010 |
| 0010 | 0011 |
| 0011 | 0001 |
| 0001 | 0000 |

**Table 2:** Experimental data table.

In conclusion, the experimental data in Figure 1 and Table 2 are the same as the data shown in the state table in Table 1 and the state diagram in Figure 2.

**Discussion and Conclusions**

By conducting the lab, it was shown that the functionality of various counters especially the 4-bit synchronous counter. From this experiment, we can see how to build counters by using JK flip-flops.

Synchronous counters use a common clock signal so that when several flip-flops must change state, the state changes occur simultaneously. A binary counter is a simple counter which counts values up when an enable signal is asserted and will reset when the reset control signal is asserted. J-K flip-flops are normally used in the synchronous counters due to the feature of the J and K inputs. There are two basic schemes for generating the J and K inputs. One of them is illustrated in the four-bit binary counter. Moreover, the information to the J-K inputs is formed in a parallel fashion. The counter is accordingly termed as synchronous parallel counter. In the parallel scheme the number of inputs to each AND gate increases linearly with the number of stages. For this added expense one gets the fastest possible synchronous counting circuit.

In this experiment, we first see how the counters are designed and how they work through simulation. Second, in our case, the experimental data matches the theoretical data by comparing the state table, state diagram and the result of our simulation. Through this comparing, we understand the function of state table/state diagram more deeply. Lastly, we grouped several flip-flops together to create sequential circuits. In our case, we use JK flip-flops to create a counter which is a kind of widely used sequential circuit. Through this, we know how to take advantages of features of different flip-flops to create a sequential circuit effectively.